CLAIMS

1. An integrated circuit comprising:

a first clock circuit delivering a first clock signal,

a second clock circuit delivering a second clock signal,

a first counting circuit for delivering a time base signal using a clock signal and a counting value, and

means for applying the first clock signal and a first counting value to the first counting circuit, so as to produce a first time base signal,

means for calculating a second counting value equal or proportional to the number of periods of the second clock signal occurring during a determined time interval equal to a period or to a whole number of periods of the first time base signal, and

means for producing a second time base signal using the second clock signal and the second counting value.

2. The integrated circuit according to claim 1 wherein the means for calculating the second counting value comprise a second counting circuit and means for applying the second clock signal to the second counting circuit during a determined time interval equal to a period or a whole number of periods of the first time base signal.

3. The integrated circuit according to claim 1 wherein the means for producing a second time base signal comprise:

the first counting circuit, and

means for applying the second counting value and the second clock signal to the first counting circuit, such that the first counting circuit produces the second time base signal.

4. The integrated circuit according to claim 3 wherein the first counting circuit is linked to a set point register receiving a counting value, and is arranged for automatically loading, at the end of a counting cycle of a counting value, the counting value present in the set point register.

5. The integrated circuit according to claim 4, comprising means for loading the second counting value into the set point register during the counting of the first counting value by the first counting circuit.

6. The integrated circuit according to claim 4 wherein the means for calculating the second counting value comprise a second counting circuit that is integrated into the set point register, and means for applying the second clock signal to the second counting circuit during a determined time interval equal to a period or a whole number of periods of the first time base signal, such that the second counting value is present in the set point register when the first counting circuit completes a counting cycle of the first counting value.

7. The integrated circuit according to claim 1 wherein the first counting circuit is a countdown counter.

8. The integrated circuit according to claim 1, comprising a multiplexer circuit for applying the first or the second clock signal to the first counting circuit.

9. The integrated circuit according to claim 1 wherein the time base signal supplied by the first counting circuit is applied to an interrupt decoder.

10. The integrated circuit according to claim 1, comprising a timer that is updated in real time sometimes in synchronisation with the first time base signal and other times in synchronisation with the second time base signal.

11. The integrated circuit according to claim 1, comprising an active halt mode during which certain elements of the integrated circuit are deactivated, the duration of which is sometimes controlled by the first time base signal and other times by the second time base signal.

12. The integrated circuit according to claim 1, comprising means for deactivating the first clock circuit while the second time base signal is produced.

13. The integrated circuit according to claim 1 wherein the first and the second clock circuits each comprise an oscillator, and wherein the oscillator of the second clock circuit features reduced current consumption and low precision relative to the oscillator of the first clock circuit.

14. The integrated circuit according to claim 1, comprising means for performing the following operations cyclically:

producing the first time base signal by means of the first counting circuit, by applying the first clock signal and the first counting value to the first counting circuit,

calibrating the second counting value while the first counting circuit is supplying the first time base signal, then

producing the second time base signal by means of the first counting circuit, by applying the second clock signal and the second counting value to the first counting circuit.

15. The integrated circuit according to claim 1, comprising a microprocessor central processing unit for driving the means for calculating the second counting value.

16. The integrated circuit according to claim 1, comprising:

a second counting circuit for calculating the second counting value,

a control register comprising a calibration bit, and

a logic circuit for applying the second clock signal to the second counting circuit during a determined time interval equal to a period or a whole number of periods of the first time base signal, when the calibration bit has a determined value.

17. The integrated circuit according to claim 16, comprising means for applying the first or the second clock signal to the first counting circuit depending on the value of a mode bit present in the control register.

18. An integrated circuit, comprising:

a first clock oscillator circuit producing a first clock signal;

a second clock oscillator circuit producing a second clock signal;

a first counting circuit coupled to the first clock oscillator circuit and to the second clock oscillator circuit and adapted to receive the first clock signal, the second clock signal and to output a first time base signal;

a logic circuit coupled to the first counting circuit and adapted to output a first counting value from the first time base signal;

a second counting circuit coupled to the second clock oscillator circuit and adapted to receive the second clock signal and output a second counting value; and

a counting value register adapted to receive and store the first counting value and the second counting value, the counting value register being coupled to the first counting circuit to provide either the first counting value or the second counting value to the first counting circuit.

19. The circuit according to claim 18, further including:

a multiplexer coupling the first clock signal to the first counting circuit; and

a connection of the second clock signal to the multiplexer, the multiplexer alternatively providing either the first clock signal or the second clock signal to the first counting circuit.